

**What is claimed is:**

- 1        1. Apparatus for use in an encoder to ensure integrity of a hypothetical decoder  
2        buffer of a video buffer verifier comprising:
  - 3            an encoder buffer including a bit content;
  - 4            a transmission controller supplied with a representation of a prescribed number of  
5        bits for controllably inhibiting transmission of bits from said encoder buffer; and  
6            a calculator for generating said representation of said prescribed number of bits in  
7        accordance with a prescribed relationship dependent on said encoder buffer bit content,  
8        and an end of picture indication.
- 1        2. The apparatus as defined in claim 1 wherein said transmission controller in  
2        response to said representation of said prescribed number of bits controllably inhibits  
3        transmission of bits from said encoder buffer upon said number of bits being read out  
4        from said encoder buffer.
- 1        3. The apparatus as defined in claim 2 wherein said calculator includes a detector  
2        for determining whether said picture has ended substantially on time.
- 1        4. The apparatus as defined in claim 3 wherein said prescribed number of bits is  
2        said encoder buffer bit content when said detector indicates that said picture ends  
3        substantially on time.
- 1        5. The apparatus as defined in claim 3 wherein said calculator is supplied with a  
2        first indication of said encoder buffer bit content when said picture actually ended and a  
3        second indication of said encoder buffer bit content when said picture should have ended.
- 1        6. The apparatus as defined in claim 5 wherein said prescribed number of bits is  
2        determined to be, in response to said first indication and said second indication, a number  
3        of bits in said encoder buffer bit content when said picture should have ended less any  
4        new bits written into said encoder buffer during an interval between when said picture  
5        actually ended to when said picture should have ended, when said detector has  
6        determined that said picture has ended early relative to an expected time for said picture  
7        to end.
- 1        7. The apparatus as defined in claim 6 wherein said encoder buffer includes a  
2        write pointer having a position representative of the number of bits written into said  
3        encoder buffer, said write pointer position at the time said picture actually ended being

4 said first indication and said write pointer position at the time said picture is expected to  
5 end being said second indication.

1       8. The apparatus as defined in claim 7 wherein said new bits written into said  
2 encoder buffer is equal to said second indication less said first indication.

1       9. The apparatus as defined in claim 3 wherein said transmission controller is  
2 essentially disabled from inhibiting transmission of bits from said encoder buffer during  
3 an interval from a time when said picture should have ended to a time when said picture  
4 actually ended, when said detector determines that said picture will end late.

1       10. The apparatus as defined in claim 9 wherein said prescribed number of bits is  
2 a number of bits in said encoder buffer bit content when said picture actually ended,  
3 when said detector has determined that said picture has ended late.

1       11. A method for use in an encoder to ensure integrity of a hypothetical decoder  
2 buffer of a video buffer verifier comprising the steps of:

3           storing bits in an encoder buffer;

4           controllably inhibiting transmission of bits from said encoder buffer in response  
5 to a representation of a prescribed number of bits; and

6           generating said representation of said prescribed number of bits in accordance  
7 with a prescribed relationship dependent on a number of bits stored in said encoder  
8 buffer, and an end of picture indication.

1       12. The method as defined in claim 11 wherein said step of controllably  
2 inhibiting, in response to said representation of said prescribed number of bits,  
3 controllably inhibits transmission of bits from said encoder buffer upon said number of  
4 bits being read out from said encoder buffer.

1       13. The method as defined in claim 12 further including a step of determining  
2 whether said picture has ended substantially on time.

1       14. The method as defined in claim 13 wherein said prescribed number of bits is  
2 said number of bits stored in said encoder buffer when said step of determining indicates  
3 that said picture ends substantially on time.

1       15. The method as defined in claim 13 wherein said step of generating utilizes a  
2 first indication of said number of bits stored in said encoder buffer when said picture

3 actually ended and a second indication of said number of bits stored in said encoder  
4 buffer when said picture should have ended.

1 16. The method as defined in claim 15 wherein said step of generating includes a  
2 step of utilizing said first indication and said second indication to generate said  
3 representation of said prescribed number of bits as being a number of bits stored in said  
4 encoder buffer when said picture should have ended less any new bits written into said  
5 encoder buffer during an interval between when said picture actually ended to when said  
6 picture should have ended, when said detector has determined that said picture has ended  
7 early relative to an expected time for said picture to end.

1 17. The method as defined in claim 16 wherein said encoder buffer includes a  
2 write pointer having a position representative of the number of bits written into said  
3 encoder buffer, said write pointer position at the time said picture actually ended being  
4 said first indication and said write pointer position at the time said picture is expected to  
5 end being said second indication.

1 18. The method as defined in claim 17 wherein said new bits written into said  
2 encoder buffer is equal to said second indication less said first indication.

1 19. The method as defined in claim 13 wherein said step of controllably  
2 inhibiting transmission is essentially disabled from inhibiting transmission of bits from  
3 said encoder buffer during an interval from a time when said picture should have ended  
4 to a time when said picture actually ended, when said step of determining determines that  
5 said picture will end late.

1 20. The method as defined in claim 19 wherein said prescribed number of bits is  
2 a number of bits in said encoder buffer bit content when said picture actually ended,  
3 when said detector has determined that said picture has ended late.